**Max Score = 15 points**

CS 250 2018 Spring Homework 01

This assignment is due at 11:59:00 pm Thursday, January 18, 2018.

Upload your typewritten answer document in either PDF or Word format to Blackboard. Download from Blackboard to be sure that your upload was successful.

Your last upload that is not marked “LATE” by Blackboard is the upload that will be graded. There is no “grace” period for late uploads

**ADVICE:** Upload your solution sufficiently before the deadline to avoid internet congestion issues and server not responding issues.

The policy for all homework assignments this semester is as follows. Please sign, which you may do by typing in your name on the signature line.

*In the following I have not represented the work of another person as my own nor have I knowingly or actively assist another person in violating this standard.*

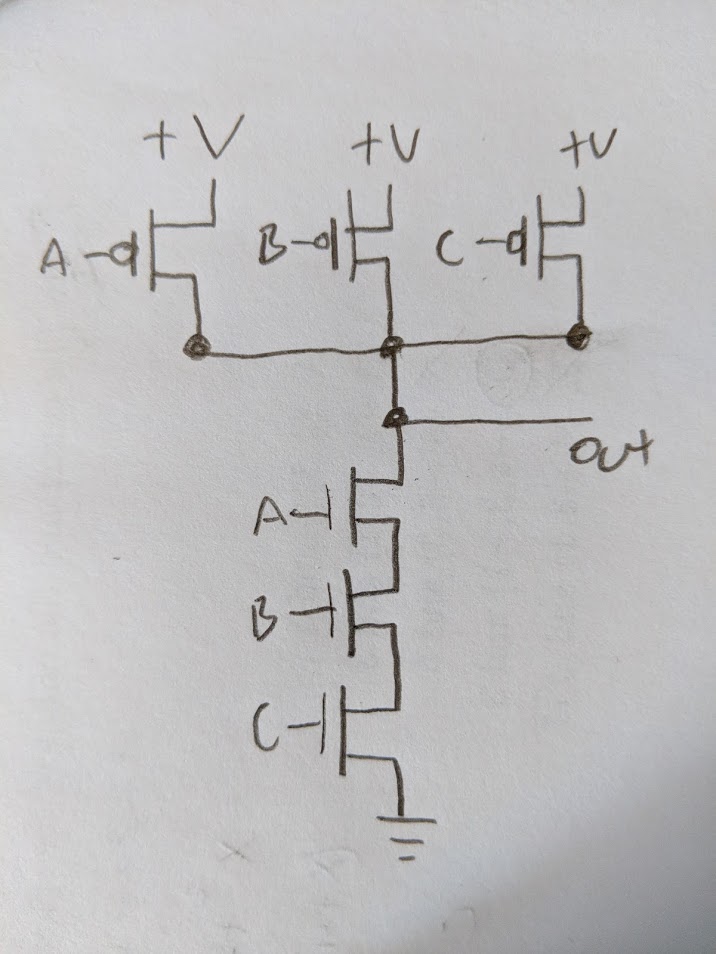
**(Signed)\_\_Connor Brown\_\_\_\_**

1. Create a single truth table that defines all possible one-input Boolean functions. At the appropriate place in the truth table give your best idea for the name of each function.

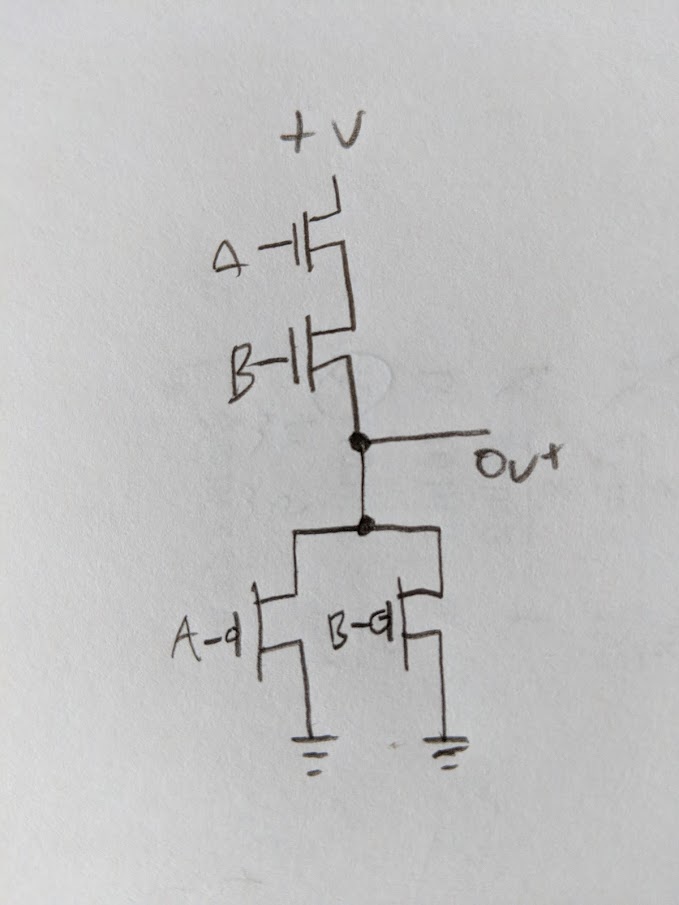
|  |  |  |  |
| --- | --- | --- | --- |
| p | ¬p | true | false |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |

1. What is the truth table for the three-input NOR(A,B,C) function? Draw the circuit for the 3-input NOR gate and the level of abstraction of the CMOS transistor. You may hand draw circuit schematics and then scan them into your document here.

|  |  |  |  |
| --- | --- | --- | --- |
| A | B | C | NOR(A,B,C) |
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 |



1. Using exactly 4 CMOS transistors, design and then draw a schematic for an AND circuit. Comment on the relationship you see between the NAND circuit presented in class and our textbook and the AND circuit that you develop.

**The difference between the NAND in class and my AND circuit is that the series path is connected to high voltage and the gates with the dot are not in a parallel path and are connected to a low voltage.**  


1. Under what conditions does a full adder generate Sum = 1 and Carry out = 0 from Augend, Addend, and Carry in? Show your answer in the form of a table.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Augend | Addend | Carry in | Sum | Carry out |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

1. What are the three key ideas behind making a circuit behave digitally?
2. It can produce two distinct output voltages.
3. It can be built to process any input voltage falling within a reasonable range as if it were the ideal value.
4. It can change the output voltage quickly so intermediate voltage values only appear briefly.
5. What principle allows for the simplification of descriptions of hardware or software by omission of detail?

**Abstraction**

1. What element in pure crystal form was used to make the first transistor?

**Germanium**

1. Why cannot a computer perform addition on the Natural numbers?

**Because there is an infinite amount of natural numbers and computers are comprised of a finite amount of hardware so therefore they cannot represent every element of the Natural number set.**